wherein a floating gate capacitance associated with the edge-defined floating gate is smaller than a control gate capacitance associated with the at least one edge-defined vertical control gate, and wherein a greater percentage of a voltage applied to the at least one vertical gate appears between the vertical floating gate and the channel region than between the at least one vertical control gate and the vertical floating gate.

7. (Amended) A transistor, comprising:

a horizontal substrate, wherein the substrate includes a source region, a drain region, and a channel region separating the source and the drain region;

an edge-defined vertical floating gate separated from a first portion of the channel region by a first oxide thickness;

at least one edge-defined vertical control gate separated from a second portion of the channel region by a second oxide thickness, wherein the at least one vertical control gate is parallel to and opposing the vertical floating gate; and

wherein a floating gate capacitance associated with the edge-defined floating gate is smaller than a control gate capacitance associated with the at least one edge-defined vertical control gate, and wherein a greater percentage of a voltage applied to the at least one vertical gate appears between the vertical floating gate and the channel region than between the at least one vertical control gate and the vertical floating gate.

14. (Amended) A floating gate transistor, comprising:

a horizontal substrate, wherein the substrate includes a source region, a drain region, and a channel region separating the source and the drain region;

a first edge-defined vertical gate located above a first portion of the channel region and separated from the channel region by a first oxide thickness;

a second edge-defined vertical gate located above a second portion of the channel region and separated from the channel region by a second oxide thickness;

a third edge-defined vertical gate located above a third portion of the channel region and separated from the channel region by the second oxide thickness; and